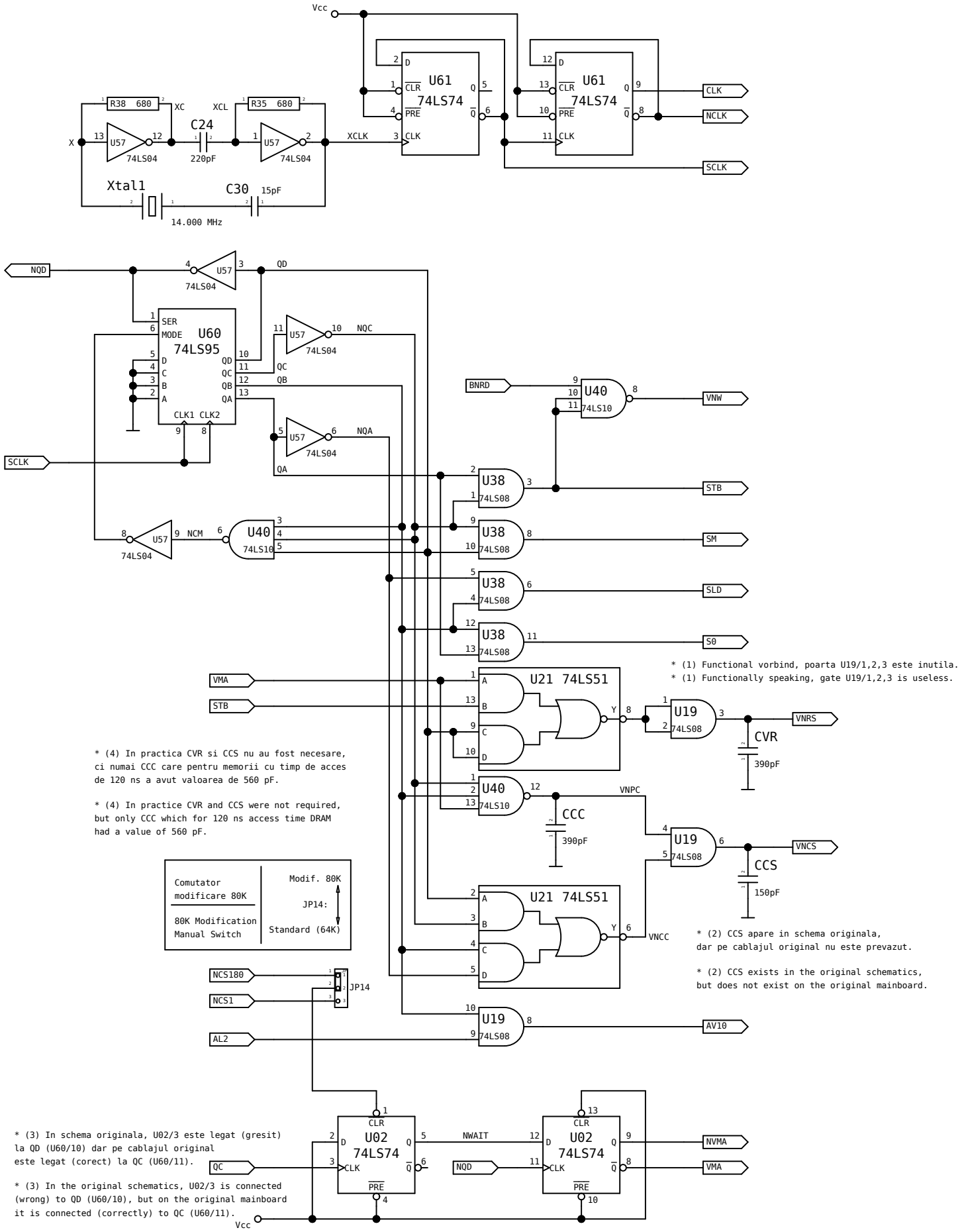


* (1) Functional vorbind, poarta U19/1,2,3 este inutila.
* (1) Functionally speaking, gate U19/1,2,3 is useless.

* (4) In practica CVR si CCS nu au fost necesare, ci numai CCC care pentru memorii cu timp de acces de 120 ns a avut valoarea de 560 pF.

* (4) In practice CVR and CCS were not required, but only CCC which for 120 ns access time DRAM had a value of 560 pF.

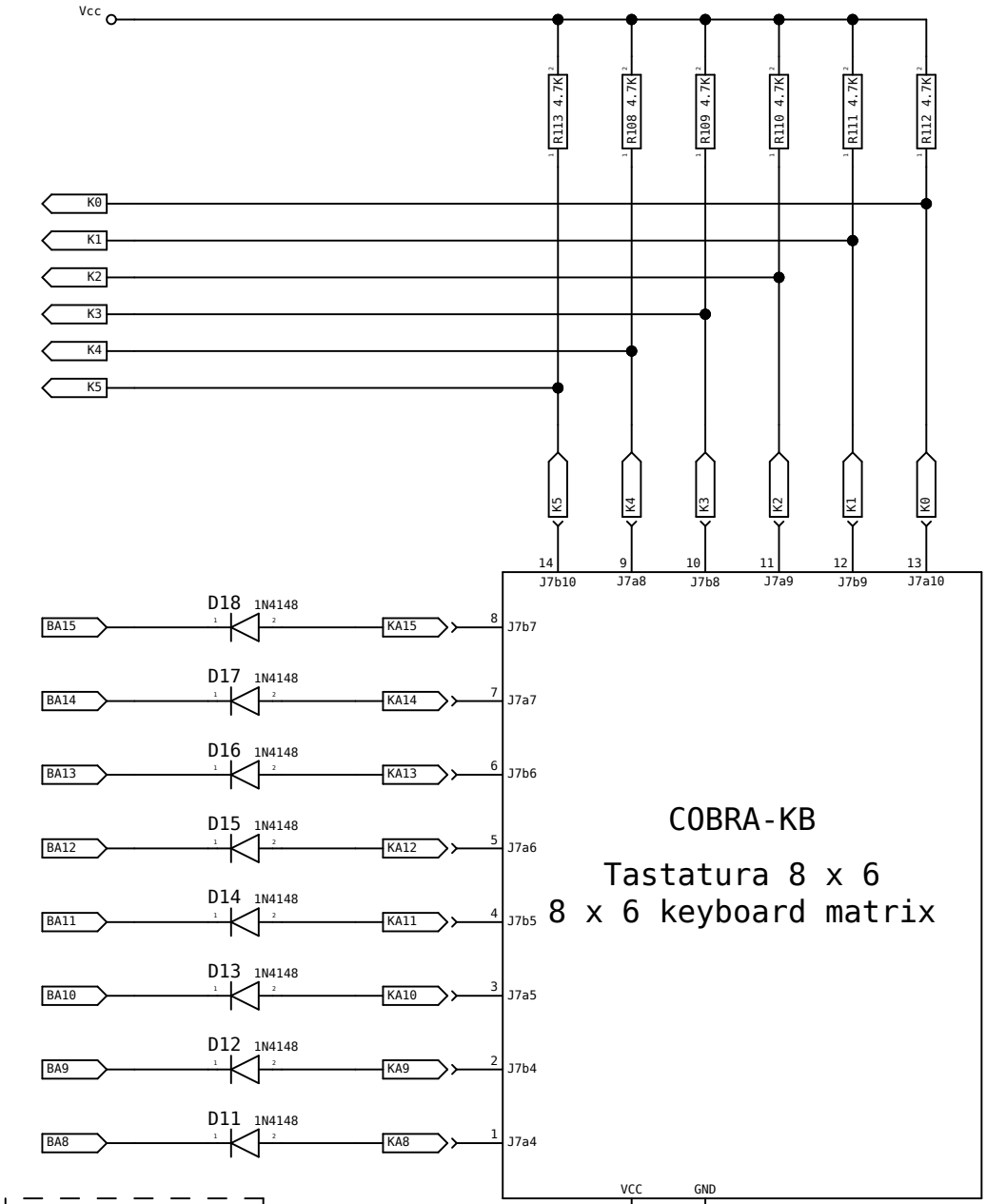
* (2) CCS apare in schema originala, dar pe cablajul original nu este prevazut.

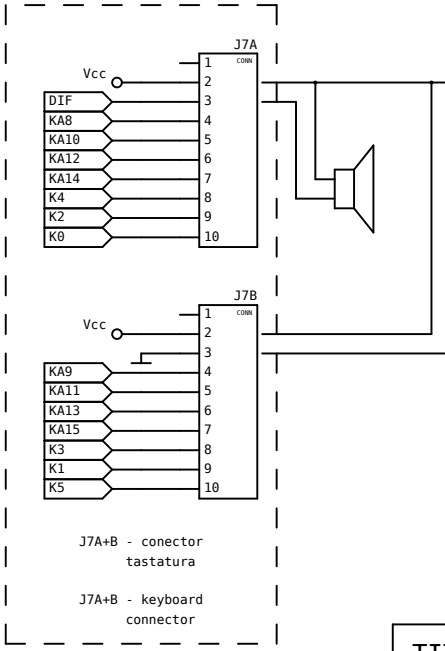
* (2) CCS exists in the original schematics, but does not exist on the original mainboard.

* (3) In schema originala, U02/3 este legat (gresit) la QD (U60/10) dar pe cablajul original este legat (corect) la QC (U60/11).

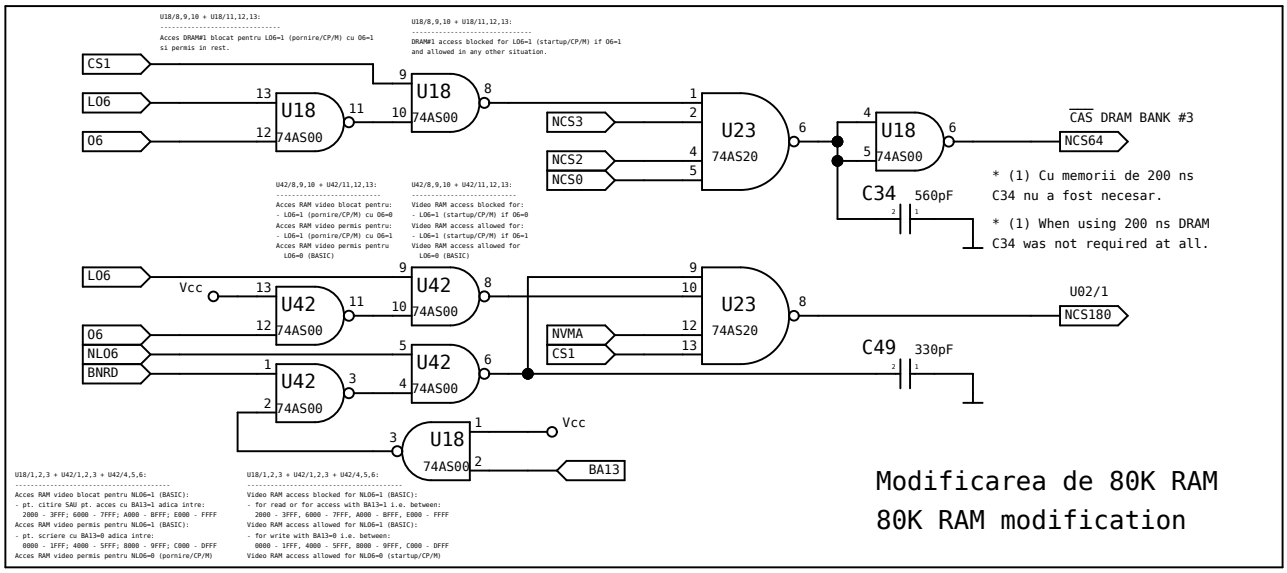
* (3) In the original schematics, U02/3 is connected (wrong) to QD (U60/10), but on the original mainboard it is connected (correctly) to QC (U60/11).

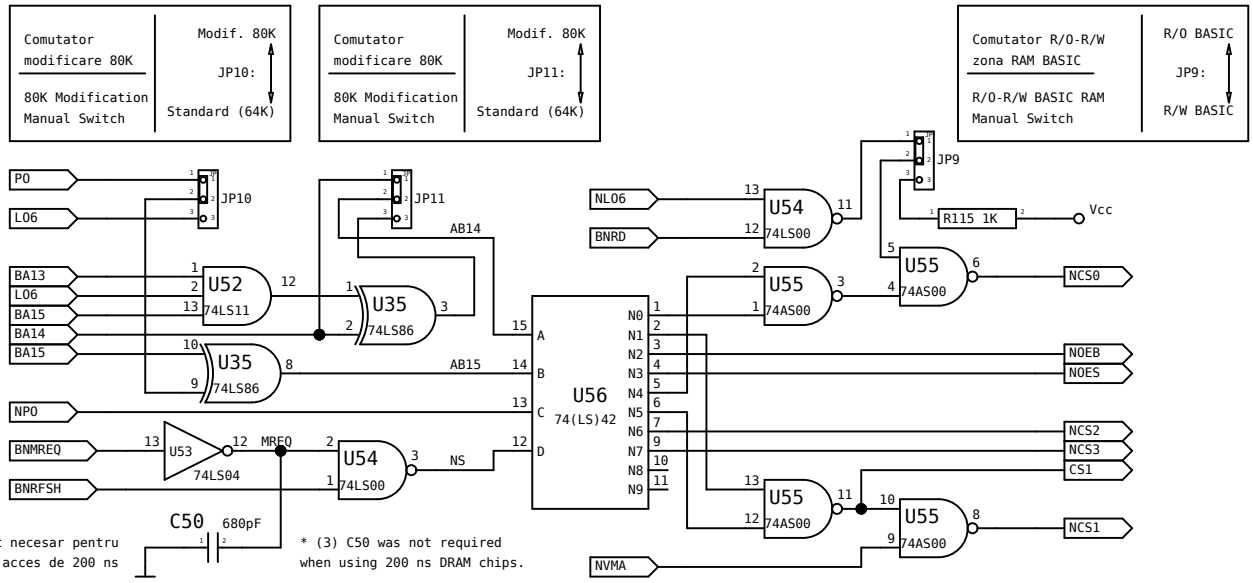
TITLE	µC CoBra - Arbitrul de memorie si logica de comanda CoBra µC - Memory access prioritizer and command logic		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	1 OF 17	DRAWN BY:	ElectroNNix





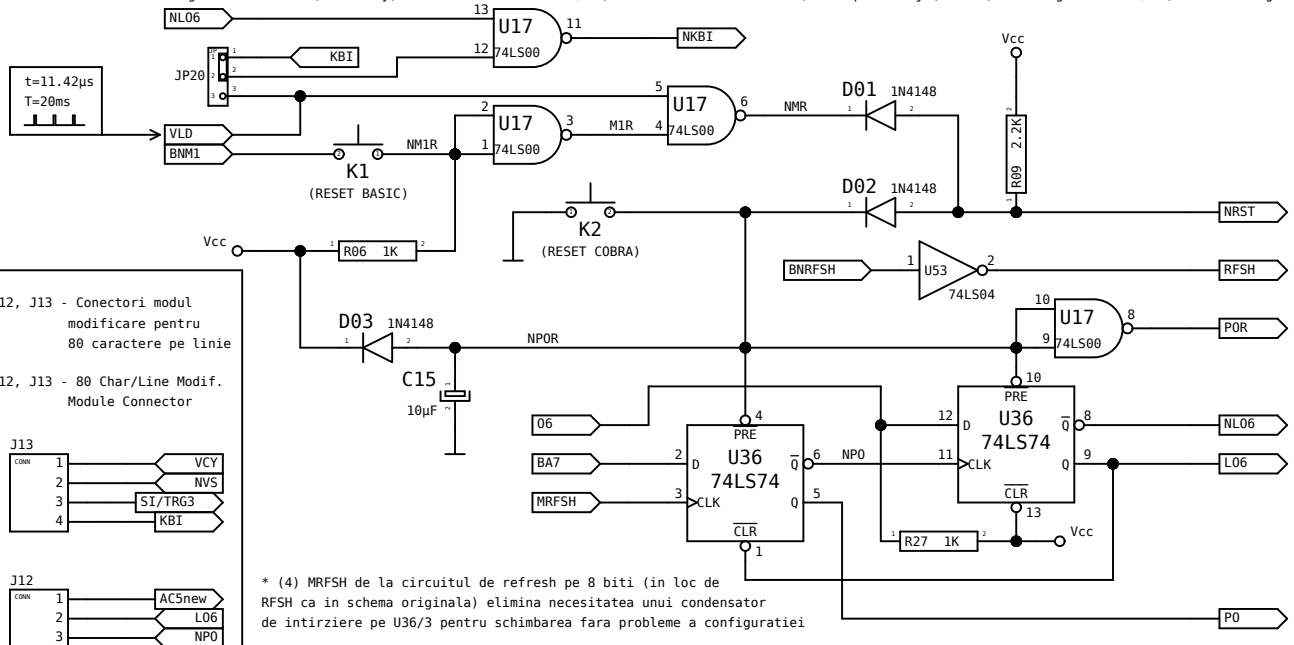
TITLE	µC CoBra - Circuitul de conectare tastatura CoBra µC - Keyboard interfacing circuit		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	2 OF 17	DRAWN BY:	ElectroNNix





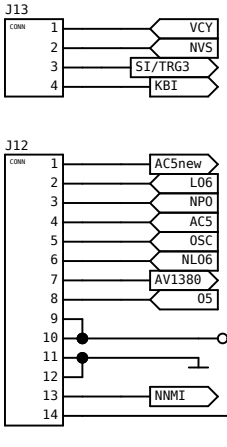
* (2) In the original schematics, input U17/12 was connected to VCY inverted through U52/6, (U52 being a 74(LS)10 (3 NOR 3-input gates)) but on the original mainboard (correctly) it is connected to U17/5 (which is connected to VLD).

* (2) In schema originala, intrarea U17/12 era legata la VCY inversat prin U52/6, (U52 fiind un 74(LS)10 (3 porti NOR cu 3 intrari)) dar pe cablaj (corect) este legata la U17/5 (care este legat la VLD).



J12, J13 - Conectori modul modificare pentru 80 caractere pe linie

J12, J13 - 80 Char/Line Modif. Module Connector



* (4) MRFSH de la circuitul de refresh pe 8 biti (in loc de RFSH ca in schema originala) elimina necesitatea unui condensator de intirziere pe U36/3 pentru schimbarea fara probleme a configuratiei

* (4) MRFSH from the 8-bit refresh circuit (instead of RFSH as in original schematics) eliminates the necessity of a delay capacitor on U36/3 for faultless change of hardware configuration

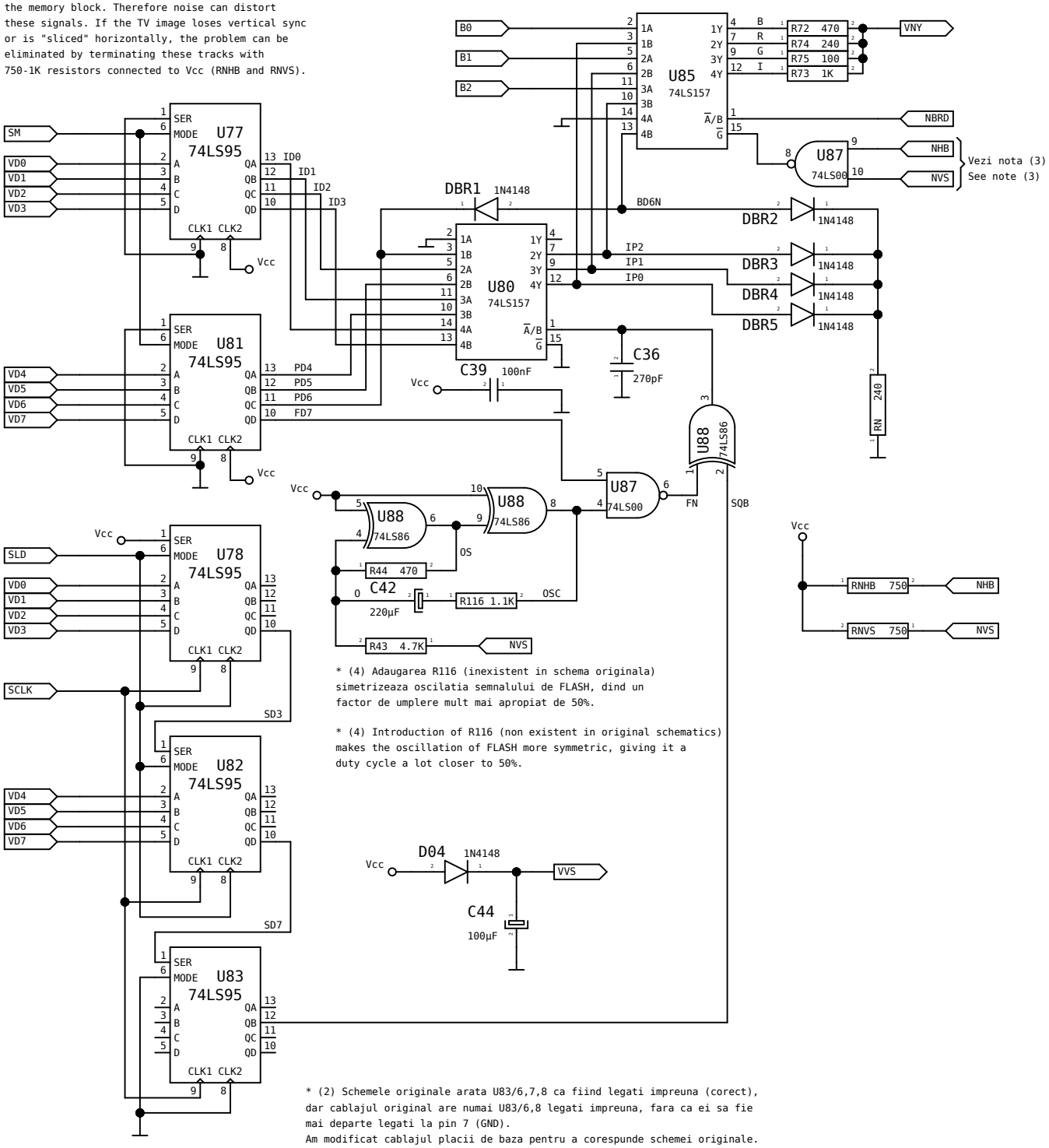
TITLE	µC CoBra - Circuitul de configurare si selectie CoBra µC - Configurator and selector circuit
FILE: CoBra	REVISION: 3.17e (test, 64/80KB DRAM)
PAGE 3 OF 17	DRAWN BY: ElectroNNix

* (3) IMPORTANT!
Semnalele NHB si NVS vin la acest circuit video
prin trasee destul de lungi, care trec prin mijlocul
blocului de memorii. De aceea e posibil sa apara
perturbatii. In caz ca imaginea se desincronizeaza
pe verticala sau se feliaza pe orizontala, situatia se
remediaza prin terminarea acestor trasee cu rezistori
de 750-1K legati la Vcc (RNHB si RNVS).

* (3) IMPORTANT!
Signals NHB and NVS get to this video circuit
through some pretty long tracks, which cross
the memory block. Therefore noise can distort
these signals. If the TV image loses vertical sync
or is "sliced" horizontally, the problem can be
eliminated by terminating these tracks with
750-1K resistors connected to Vcc (RNHB and RNVS).

* (1) In schema originala, diodele DBR1-5 si rezistenta RN sint desenate
(cu toate ca diodele nu sint denumite) dar pe cablajul original nu sint prevazute,
iar U85/13 este legat direct la U80/3. Ca urmare, cablajul original nu permitea
functia de BRIGHT. Am modificat cablajul adaugind gauri pentru BDR1-5 si RN
si intrerupind deci legatura directa dintre U85/13 si U80/3.

* (1) In the original schematics, diodes DBR1-5 and resistor RN are drawn
(although the diodes don't have names) but on the original mainboard they are not placed,
and U85/13 is directly connected to U80/3. Therefore, the original mainboard would not
allow the BRIGHT function. I have modified the mainboard layout by adding mounting holes for
BDR1-5 and RN and therefore interrupting the direct connection between U85/13 and U80/3.



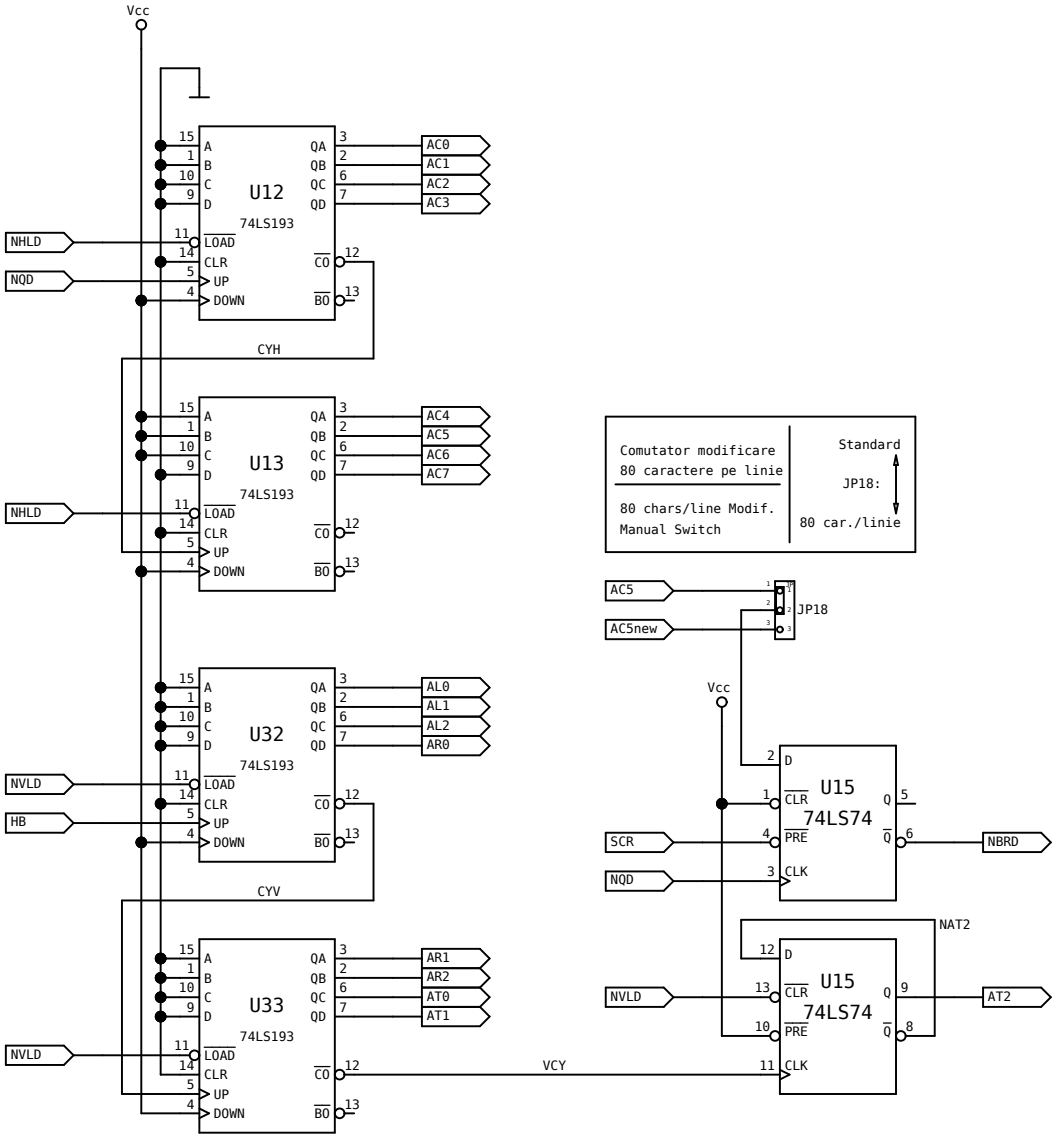
* (4) Adaugarea R116 (inexistent in schema originala)
simetrizeaza oscilatia semnalului de FLASH, dind un
factor de umplere mult mai apropiat de 50%.

* (4) Introduction of R116 (non existent in original schematics)
makes the oscillation of FLASH more symmetric, giving it a
duty cycle a lot closer to 50%.

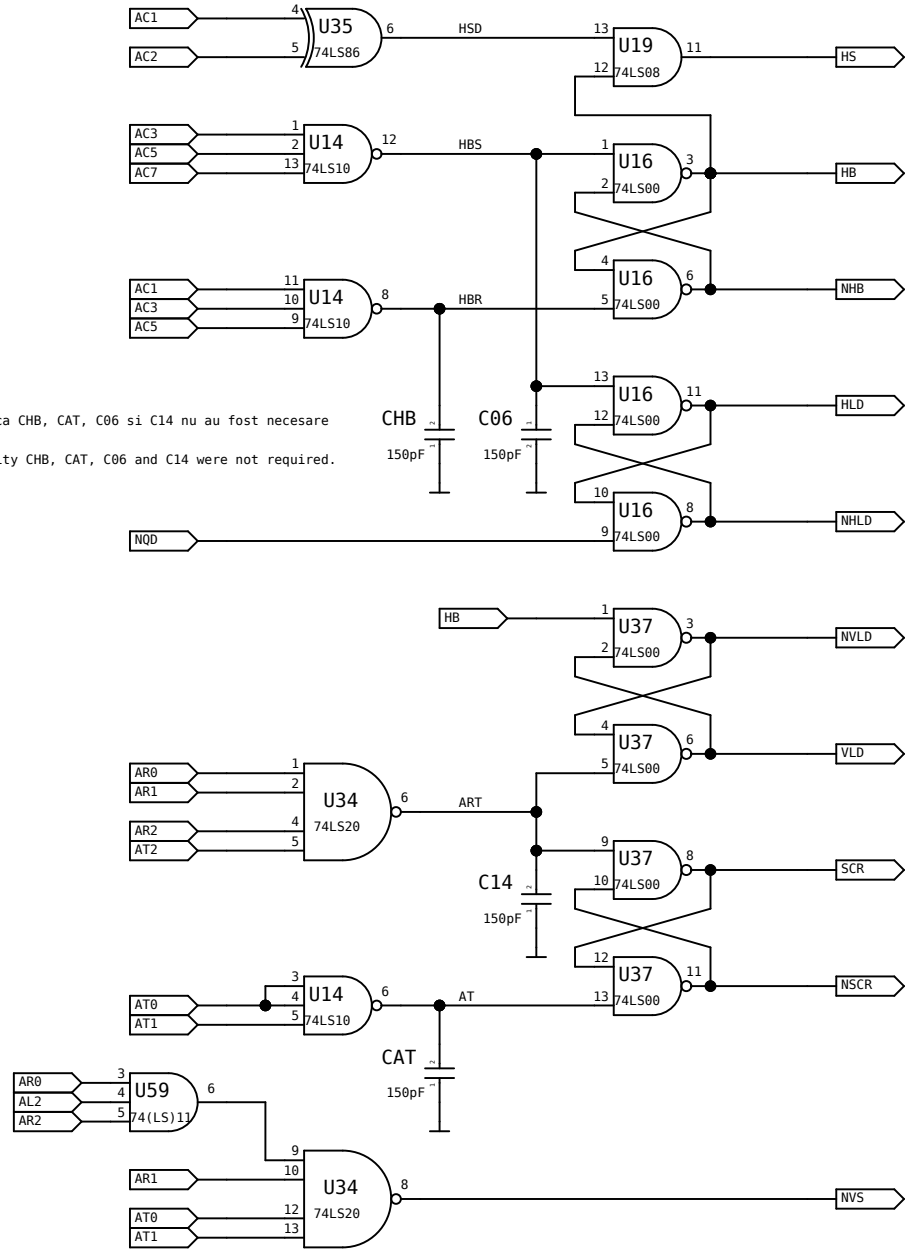
* (2) Schemele originale arata U83/6,7,8 ca fiind legati impreuna (corect),
dar cablajul original are numai U83/6,8 legati impreuna, fara ca ei sa fie
mai departe legati la pin 7 (GND).
Am modificat cablajul placii de baza pentru a corespunde schemei originale.
(Vezi legatura #25 fata 2)

* (2) The original schematics show U83/6,7,8 connected together (correctly),
but the original mainboard layout only has U83/6,8 connected together
without them being further connected to pin 7 (GND).
I have modified the mainboard layout to match the original schematics.
(See rewiring #25 side 2)

TITLE	µC CoBra - Circuitul formator semnal video CoBra µC - Video signal generator circuit
FILE: CoBra	REVISION: 3.17e (test, 64/80KB DRAM)
PAGE 4 OF 17	DRAWN BY: ElectroNNix



TITLE	µC CoBra - Circuitul de generare adrese video CoBra µC - Video address generator circuit		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	5 OF 17	DRAWN BY:	ElectroNNix



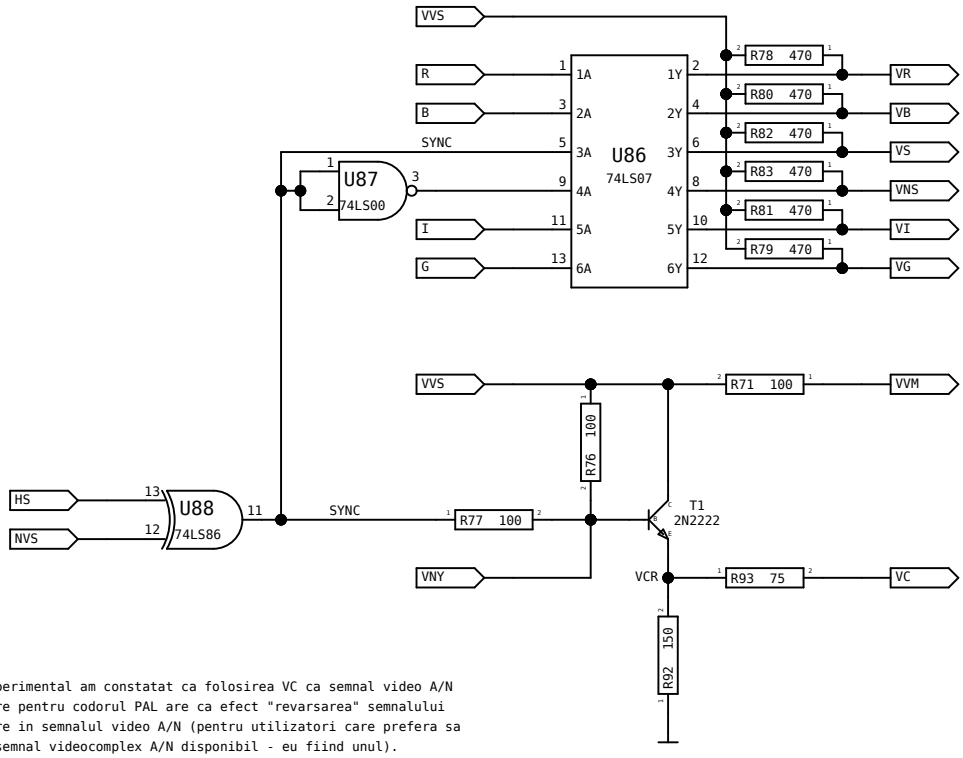
* (1) In practica CHB, CAT, C06 si C14 nu au fost necesare

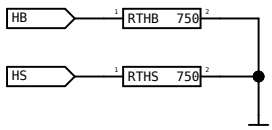
* (1) In actuality CHB, CAT, C06 and C14 were not required.

* (2) Poarta U59/6 inlocuieste AR2 din schema originala cu un produs de 3 semnale in scopul aducerii impulsului de sincro cadre mai aproape de durata standard.

* (2) Gate U59/6 replaces AR2 in the original schematics with an AND of 3 signals for the purpose of bringing the vertical sync pulse closer to the standard duration.

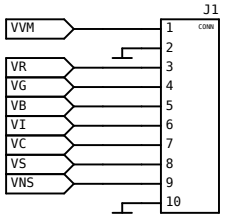
TITLE	µC CoBra - Circuitul generator de sincroimpulsuri CoBra µC - Video sync pulses generator circuit
FILE: CoBra	REVISION: 3.17e (test, 64/80KB DRAM)
PAGE 6 OF 17	DRAWN BY: ElectroNNix





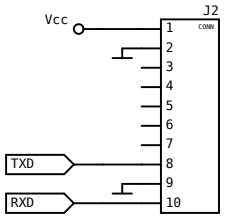
J1 - CONECTOR VIDEO

J1 - VIDEO CONNECTOR



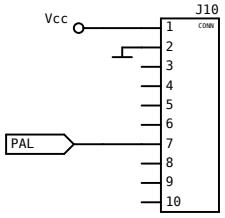
J2 - CONECTOR RS232

J2 - RS232 CONNECTOR



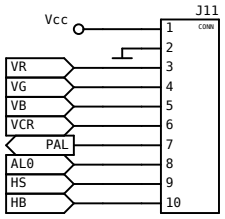
J10 - CONECTOR PAL VIDEO

J10 - PAL VIDEO CONNECTOR



J11 - CONECTOR CODOR PAL

J11 - PAL CODER CONNECTOR



* (1) Experimental am constatat ca folosirea VC ca semnal video A/N
de intrare pentru codorul PAL are ca efect "revarsarea" semnalului
de culoare in semnalul video A/N (pentru utilizatori care prefera sa
aiba si semnal videocomplex A/N disponibil - eu fiind unul).
Asa ca pentru semnal de intrare in codorul PAL am folosit VCR in loc de VC.

* (1) While experimenting I noticed that using VC as B/W video input
to the PAL coder has the unwanted side effect of color "spillover" into the
B/W video output (for those users who still prefer having B/W video output
available - me being one of them).
So instead of VC as input to the PAL coder I used VCR.

* (2) IMPORTANT!
Semnalele HB si HS vin la acest circuit video prin trasee destul de lungi,
(HS trece prin mijlocul blocului de memorii). De aceea e posibil sa apara
perturbatii. In caz ca imaginea se feliaza pe orizontala, situatia se
remediaza prin terminarea acestor trasee cu rezistori de 750-1K
legati la GND (RTHB si RTHS). Vezi si nota (3) de la circuitul formator
semnal video (pag. 4) pentru semnalul NVS.

* (2) IMPORTANT!
Signals HB and HS arrive to this video circuit through pretty long
tracks, (HS crosses the memory block). Therefore noise can distort
this signal. If the TV image is "sliced" horizontally, the problem
can be eliminated by terminating these track with 750-1K resistors
connected to GND (RTHB and RTHS). See also note (3) at page 4,
(the Video Signal Generator Circuit), regarding signal NVS.

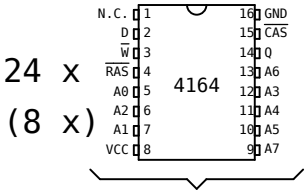
TITLE	µC CoBra - Circuitul de interfata cu monitorul TV CoBra µC - TV monitor interfacing circuit
FILE: CoBra	REVISION: 3.17e (test, 64/80KB DRAM)
PAGE 7 OF 17	DRAWN BY: ElectroNNix

* (2) In practica am facut teste cu doua tipuri de memorii: cu timp de acces de 120 ns si de 200 ns. Experimental am constatat ca pentru timpi de acces mari (200 ns) U41 si U58 trebuie sa fie 74S157 (timp de propagare mic), iar pentru timpi de acces mici (120 ns) trebuie sa fie 74LS157 (timp de propagare mare). Totusi memoriile de 120 ns n-au functionat corect in nici un caz in cadrul acestui circuit de memorie sistem. Concluzia: acest circuit necesita memorii DRAM cu timp de acces mare (150-200 ns, 200 ns e valoarea optima).

* (2) Practically I did tests with 2 types of memories: 120 ns and 200 ns access time. Experimentally I found that for high acces times (200 ns) U41 and U58 must be 74S157 (low propagation time), and for low access times (120 ns) they must be 74LS157 (high propagation time). Yet the 120 ns memories never worked properly. Conclusion: this circuit requires DRAM memories with high access time (150-200 ns, 200 ns would be the optimal value).

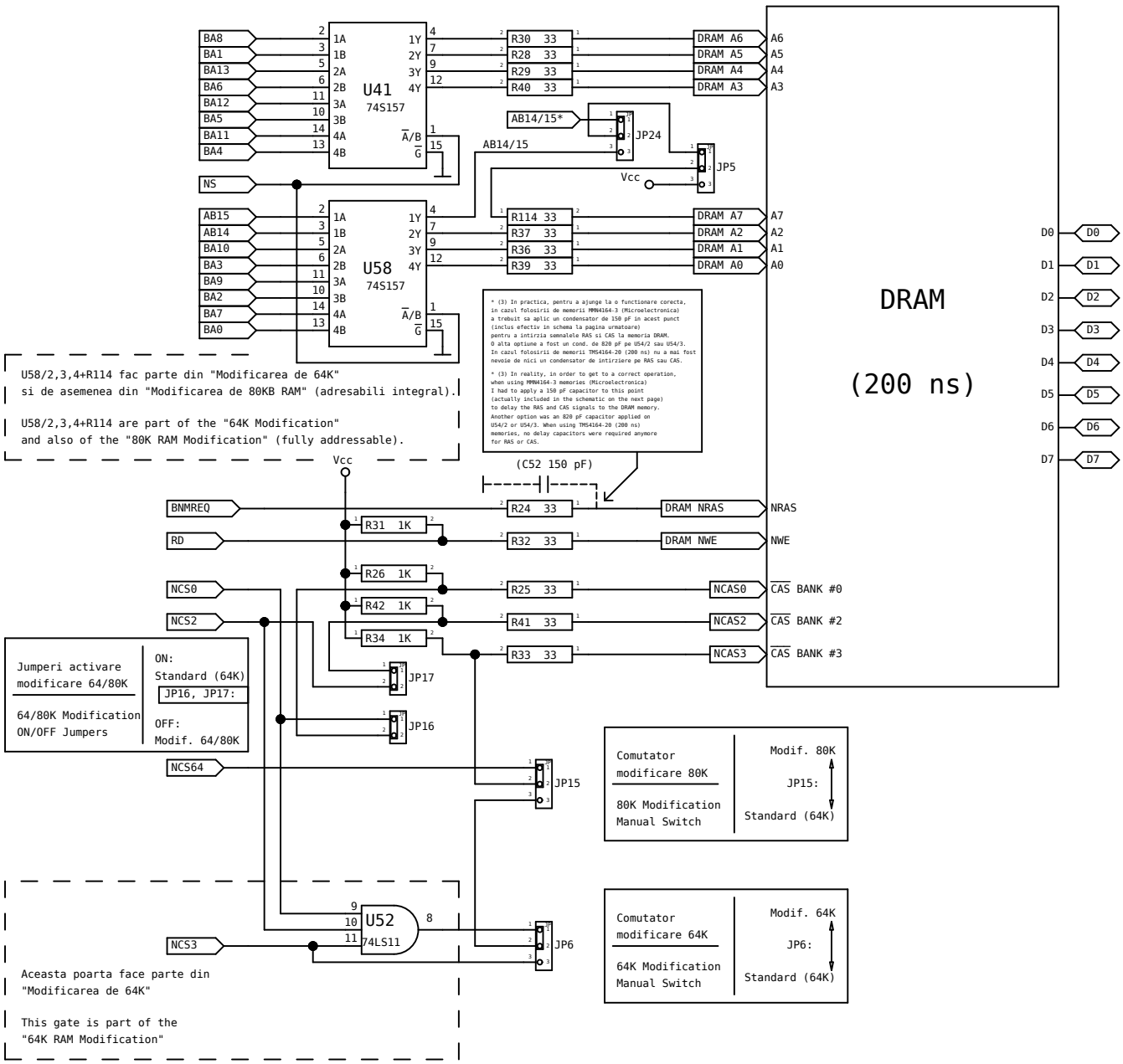
* (1) Memorii de 64K x 1 bit.
In configuratia standard sint folosite ca memorii de 16K x 1 bit (A7 legat la VCC) si toate bancurile (0, 2, 3) sint ocupate (24 cipuri folosite). In configuratia modificarii de 64K sau 80K, linia de adresa A7 este folosita si numai bancul 3 este ocupat (8 cipuri folosite).

* (1) 64K x 1 bit memories.
In standard configuration they are used as 16K x 1 bit memories (A7 kept at "1") and all memory banks (0, 2, 3) are used (24 chips used). In the "64K / 80K Modification" configuration, DRAM address line A7 is used and only memory bank 3 is used (8 memory chips used).



Jumper refresh DRAM pe 7biti/8biti
7-bit/8-bit DRAM Refresh Jumper
8-bit Refresh
JP24:
7-bit Refresh

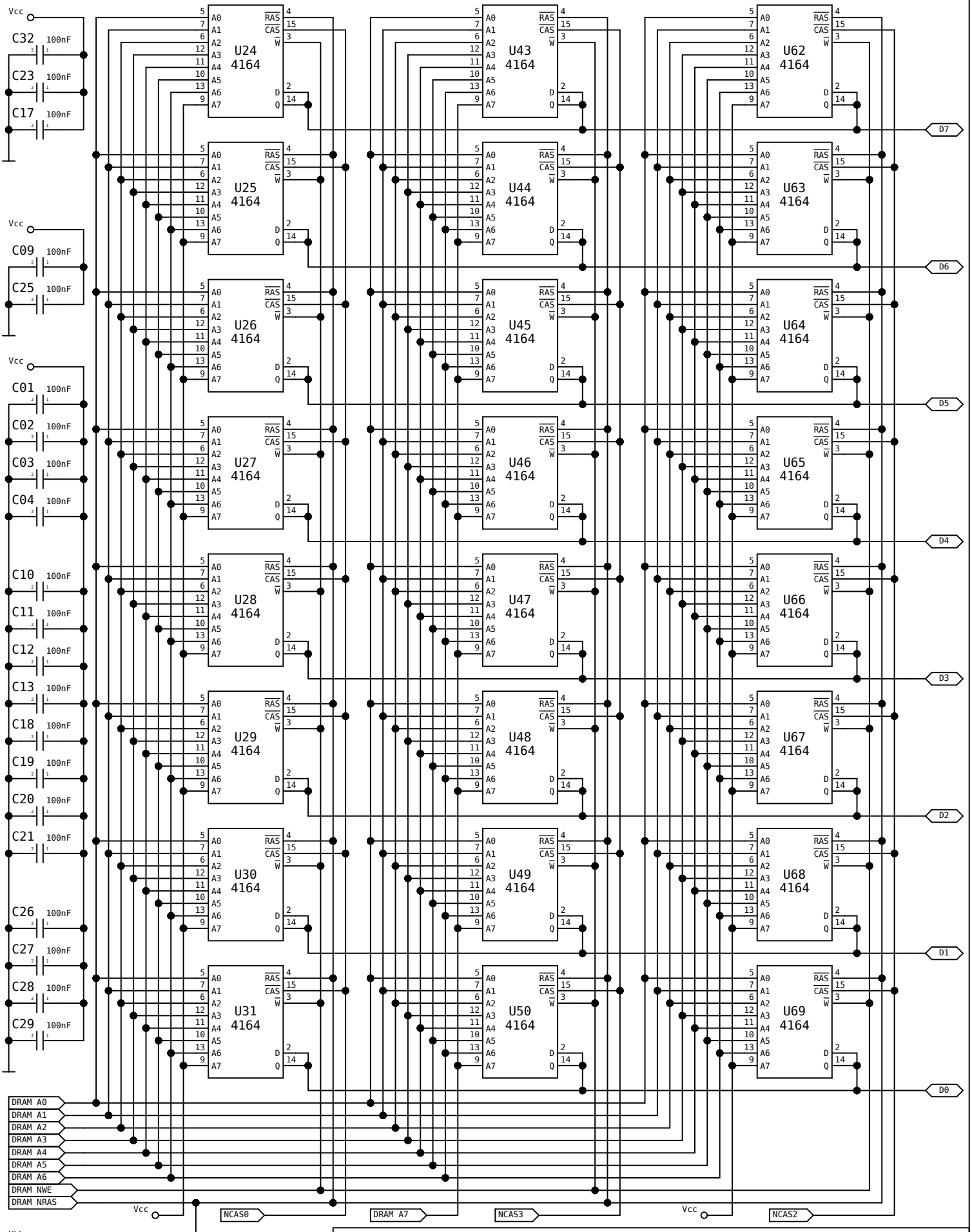
Comutator modificare 64/80K
64/80K Modification Manual Switch
Modif. 64/80K
JP5:
Standard (64K)



* (3) In practica, pentru a ajunge la o functionare corecta, in cazul folosirii de memorii MMN4164-3 (Microelectronica) a trebuit sa aplic un condensator de 150 pF in acest punct (inclus efectiv in schema la pagina urmatoare) pentru a intirzia semnalele RAS si CAS la memoria DRAM. O alta optiune a fost un cond. de 820 pF pe U54/2 sau U54/3. In cazul folosirii de memorii TMS4164-20 (200 ns) nu a mai fost nevoie de nici un condensator de intirziere pe RAS sau CAS.

* (3) In reality, in order to get to a correct operation, when using MMN4164-3 memories (Microelectronica) I had to apply a 150 pF capacitor to this point (actually included in the schematic on the next page) to delay the RAS and CAS signals to the DRAM memory. Another option was an 820 pF capacitor applied on U54/2 or U54/3. When using TMS4164-20 (200 ns) memories, no delay capacitors were required anymore for RAS or CAS.

TITLE	µC CoBra - Circuitul memoriei dinamice - pag.1/2 CoBra µC - Dynamic memory circuit - pag.1/2		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	8 OF 17	DRAWN BY:	ElectroNNix



* (1) Cu memorii de 200 ns, C52 nu a fost necesar.

* (1) For 200 ns DRAM, C52 was not required at all.

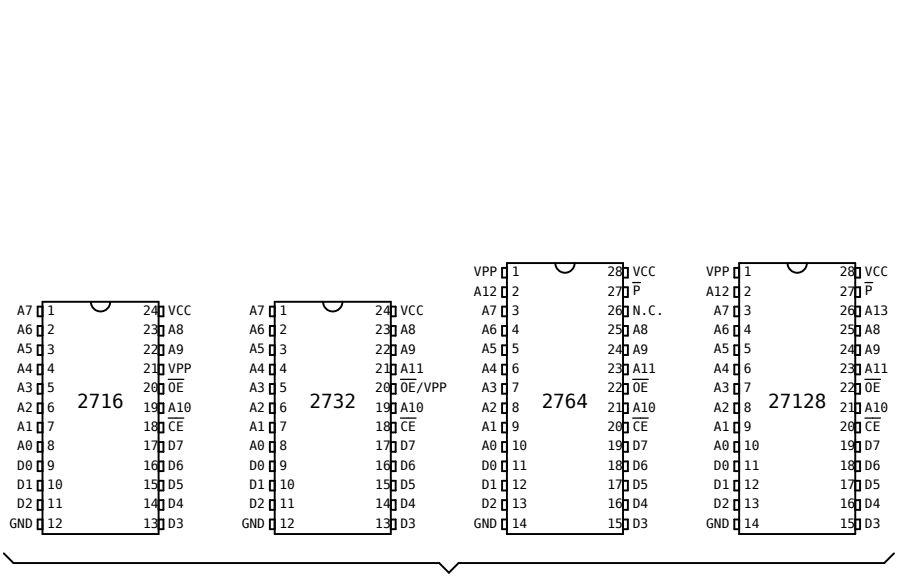
TITLE μC CoBra - Circuitul memoriei dinamice - pag.2/2
CoBra μC - Dynamic memory circuit - pag.2/2

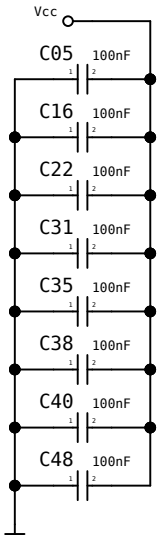
FILE: CoBra

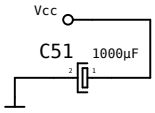
REVISION: 3.17e (test, 64/80KB DRAM)

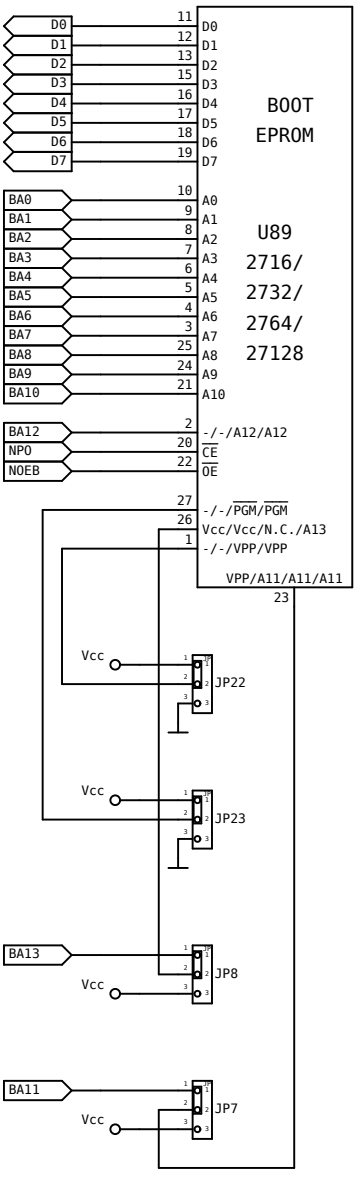
PAGE 9 OF 17

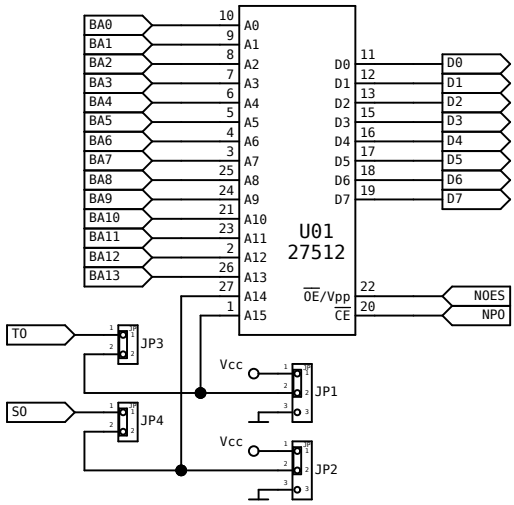
DRAWN BY: ElectroNNix











* (3) JP22 si JP23 dau posibilitatea folosirii unui 27512 ca EPROM BOOT cu selectia uneia din cele 4 zone de 16KB ca zona de EPROM BOOT folosita in mod curent.

* (3) JP22 si JP23 offer the choice of using a 27512 as BOOT EPROM by selecting one 16KB memory area as the BOOT area currently used.

SELECTIE ADR. EPROM BOOT PENTRU 27512	JP22: (A15) "1" / "0"
ADDR. SELECT BOOT EPROM FOR 27512	JP23: (A14) "1" / "0"

SELECTIE TIP EPROM (BOOT)	JP8: 27128 / 2716/32/64
EPROM type selector (BOOT)	JP7: 2732/64/128 / 2716

* (2) JP1 si JP3 folosesc acelasi jumper care este pus la un moment dat ori peste doi din pinii lui JP1, ori peste pinii lui JP3. Atunci cind este pus pe pinii lui JP1, comuta (manual) adresa A15 la "1" sau "0" logic, iar atunci cind este pus pe JP3, adresa A15 a BASIC EPROM este comandata prin software (din BOOT EPROM in configuratia de pornire) cu semnalul TO. Acelasi lucru se intimpla cu JP2 si JP4 si semnalul SO.

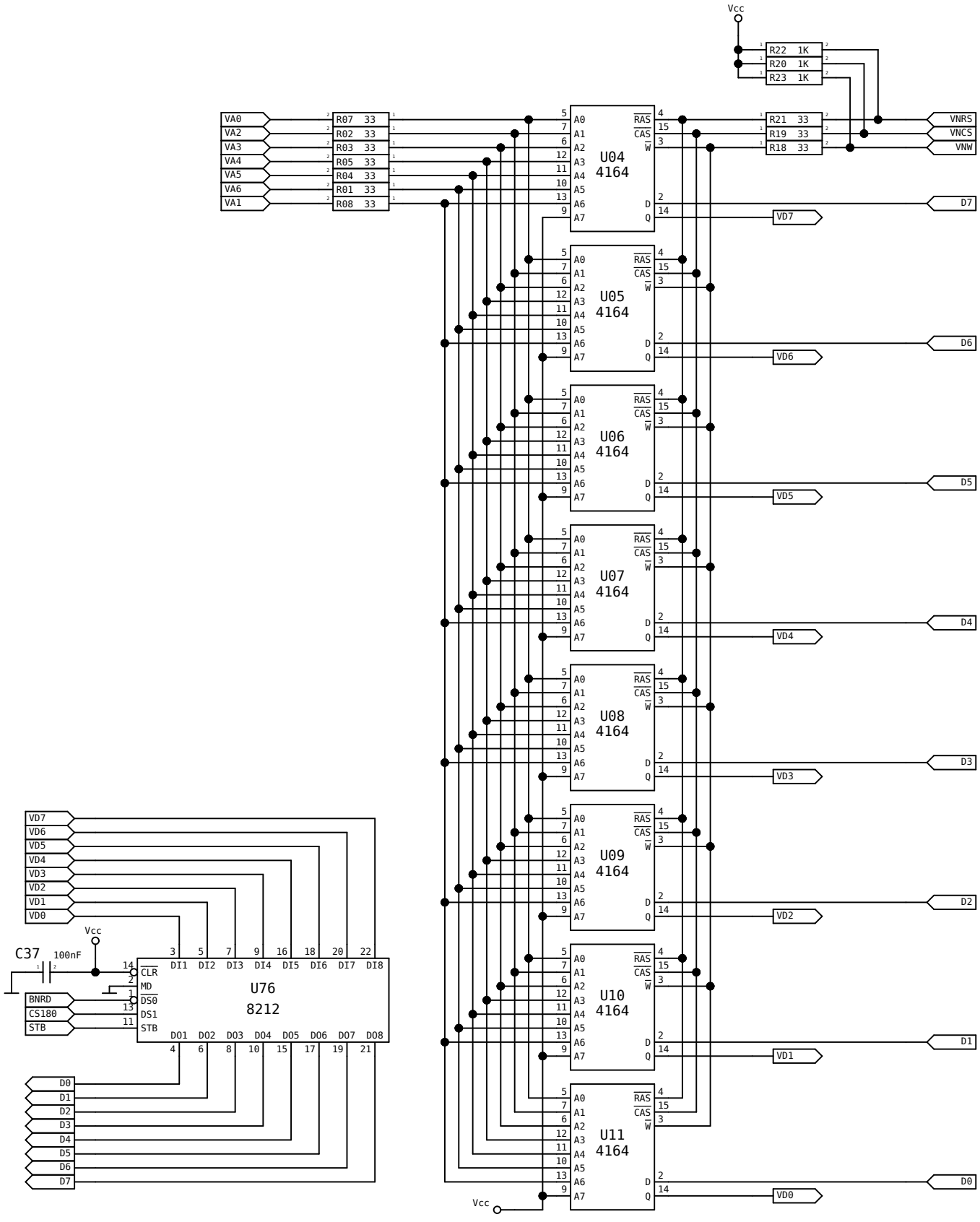
* (2) JP1 and JP3 use the same jumper which at a given moment is either sitting on two of JP1's pins or is sitting on JP3. When seated on JP1, it (manually) switches address line A15 to a "1" or "0" level and when on JP3 the address line A15 of BASIC EPROM is software controlled (by the code in the BOOT EPROM in the startup configuration) with the TO signal. The same thing happens with JP2 and JP4 and the SO signal.

	2716	2732	2764	27128	27256	27512
JP7	2-3	1-2	1-2	1-2	1-2	1-2
JP8	2-3	2-3	2-3	1-2	1-2	1-2

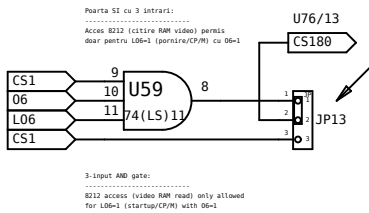
TITLE µC CoBra - Circuitul memoriei nevolatile
CoBra µC - Read-only memory circuit

FILE: CoBra | REVISION: 3.17e (test, 64/80KB DRAM)

PAGE 10 OF 17 | DRAWN BY: ElectroNNix



Acest circuit face parte din "Modificarea de 80KB RAM" (adresabili integral).



This circuit is part of the "80K RAM Modification" (fully addressable).

Comutator modificare 80K

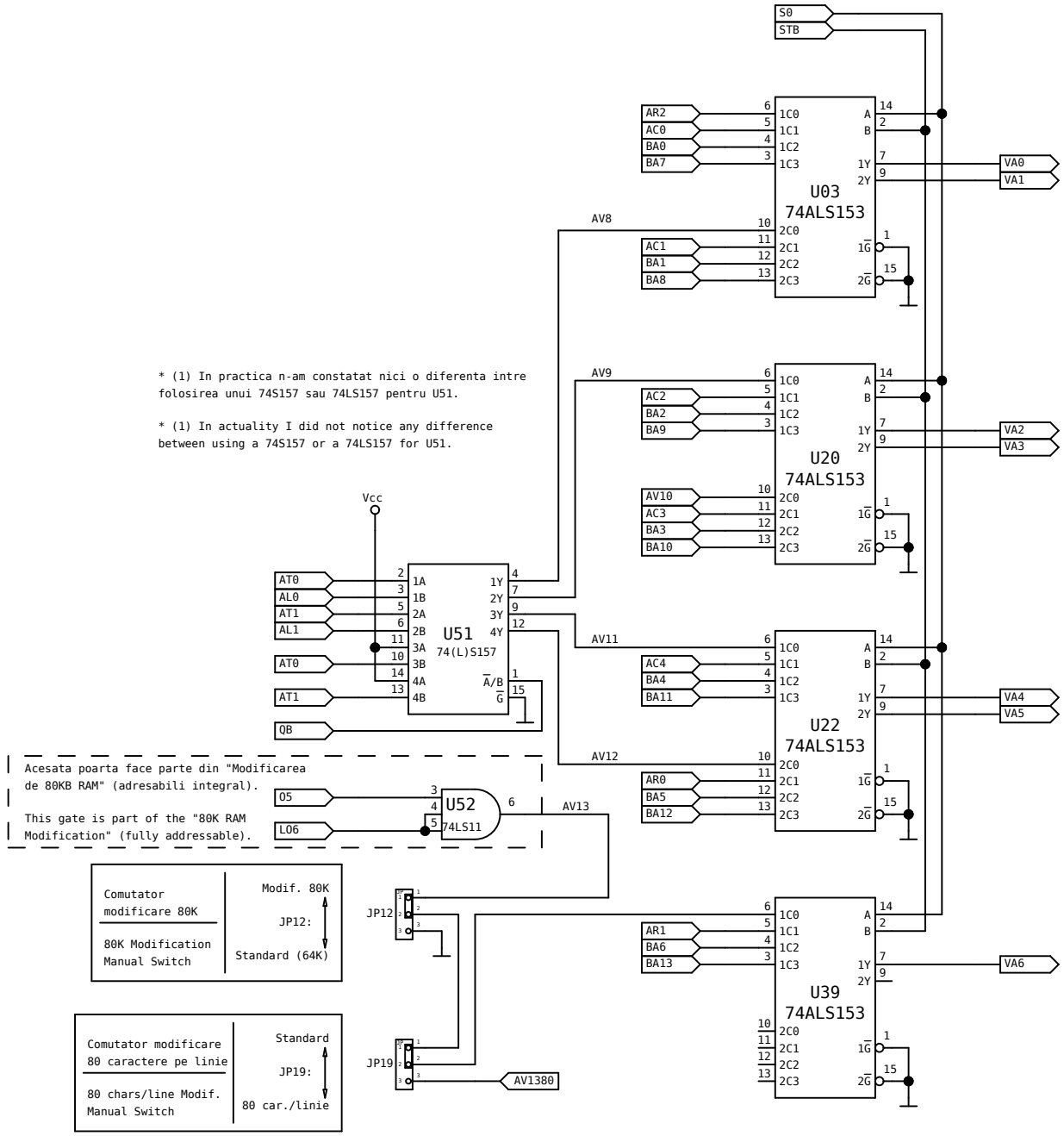
80K Modification Manual Switch

Modif. 80K

JP13:

Standard (64K)

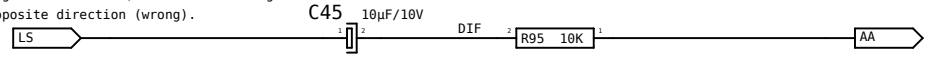
TITLE	µC CoBra - Circuitul memoriei video CoBra µC - Video memory circuit		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	11 OF 17	DRAWN BY:	ElectroNNix



TITLE	µC CoBra - Circuitul de multiplexare adrese video CoBra µC - Video address multiplexer circuit		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	12 OF 17	DRAWN BY:	ElectroNNix

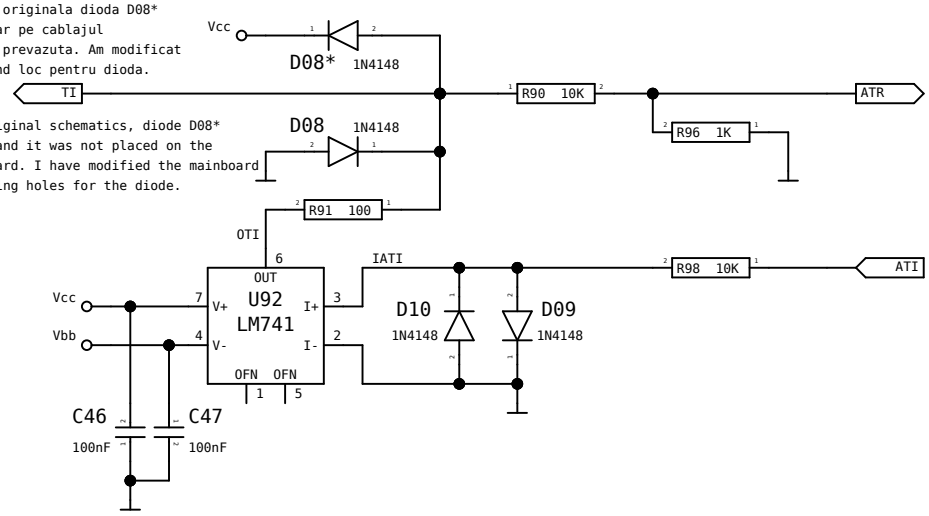
* (1) In schema originala semnalele
LS si AA erau desenate in sens opus (gresit).

* (1) In the original schematics, the LS and AA signals
were drawn in opposite direction (wrong).



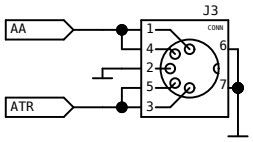
* (2) In schema originala dioda D08*
nu avea nume, iar pe cablajul
original nu era prevazuta. Am modificat
cablajul adaugind loc pentru dioda.

* (2) In the original schematics, diode D08*
was not named, and it was not placed on the
original mainboard. I have modified the mainboard
by adding mounting holes for the diode.



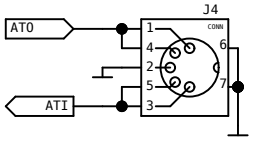
J3 - CONECTOR AUXILIAR

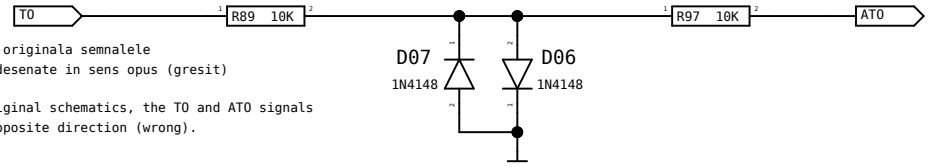
J3 - AUX CONNECTOR



J4 - CONECTOR CASETOFON

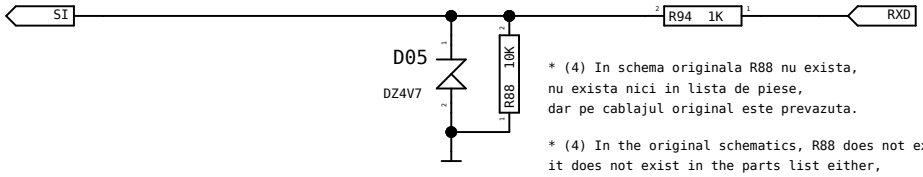
J4 - TAPE CONNECTOR





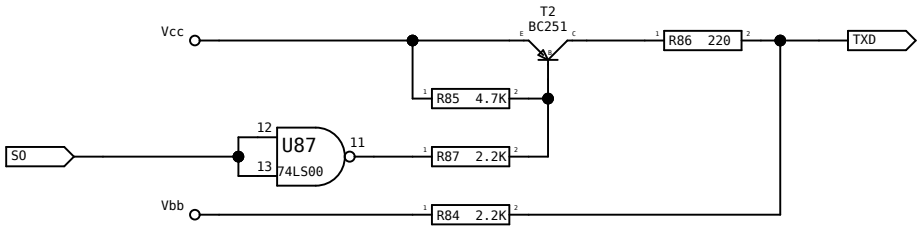
* (3) In schema originala semnalele
TO si ATO erau desenate in sens opus (gresit)

* (3) In the original schematics, the TO and ATO signals
were drawn in opposite direction (wrong).



* (4) In schema originala R88 nu exista,
nu exista nici in lista de piese,
dar pe cablajul original este prevazuta.

* (4) In the original schematics, R88 does not exist,
it does not exist in the parts list either,
but it is placed on the original mainboard.

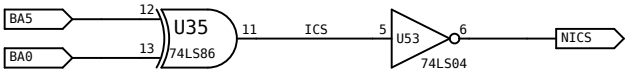


* (5) Pe cablajul original, poarta U87/13,12,11
era intercalata ca inversor intre U85/12 si U86/11,
inversind semnalul I de la U85 la U86 (gresit). Am modificat
deci cablajul conform acestei scheme (originale, corecte).
(Vezi taieturile #1 si #2 de pe fata 1, #20 si #24 de pe fata 2,
si legaturile #18, #20 si #21 de pe fata 2)

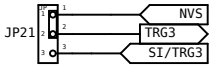
* (5) On the original PCB, gate U87/13,12,11 was
placed as inverter between U85/12 and U86/11,
inverting the signal I from U85 to U86 (wrong). I have
therefore changed the mainboard layout according to
the original (correct) schematic (shown here).
(See cuts #1 & #2 on side 1, #20 & #24 on side 2,
and rewirings #18, #20 & #21 on side 2)

TITLE µC CoBra - Circuite de adaptare nivel CoBra µC - Voltage-level adapter circuits	
FILE: CoBra	REVISION: 3.17e (test, 64/80KB DRAM)
PAGE 13 OF 17	DRAWN BY: ElectroNNix

* (1) Pe cablajul original JEXA/8 este legat in mod gresit la BA7.
De asemenea, manualul original avea JEXA/8 listat ca fiind
legat la BA7. Am modificat deci cablajul si
schema de fata legind JEXA/8 la BA1 (corect).
(Vezi taietura #11 fata 1, legatura #22 fata 2)

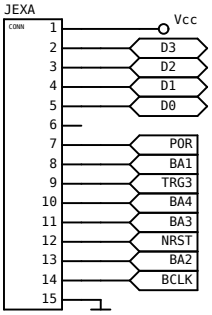


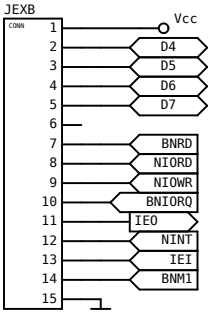
* (1) On the original mainboard, JEXA/8 was connected (the wrong way)
to BA7. Also the original hardware manual had JEXA/8 listed as being
connected to BA7.
I have therefore changed the mainboard layout and
this schematic by connecting JEXA/8 to BA1 (correctly).
(See cut #11 side 1, rewiring #22 side 2)



JEXA+B - CONECTOR INTERFATA
FLOPPY DISK

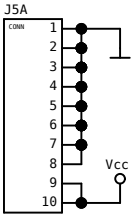
JEXA+B - FLOPPY DISK INTERFACE
CONNECTOR

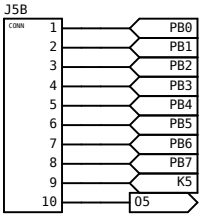




J5A+B - CONECTOR PORT INTRARE
PE 8 BITI ADRESA 0DFH

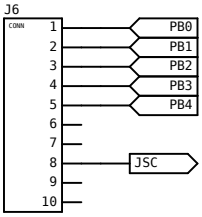
J5A+B - 8-BIT INPUT PORT 0DFH
CONNECTOR

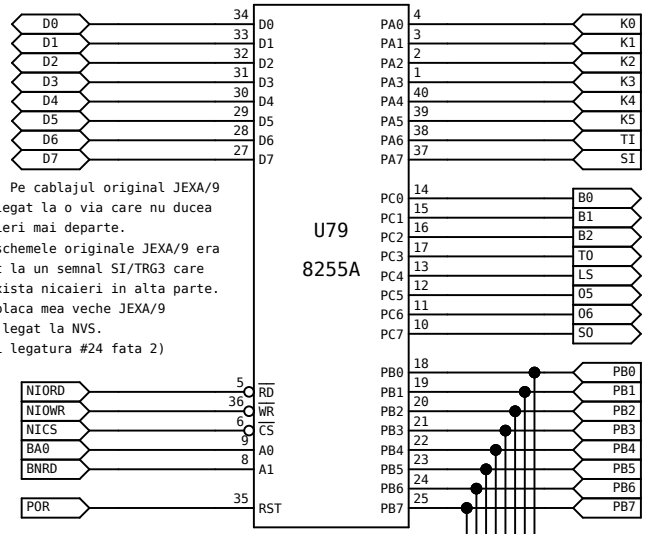




J6 - CONECTOR JOYSTICK
KEMPSTON

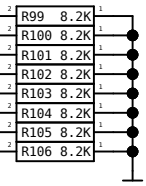
J6 - KEMPSTON JOYSTICK
CONNECTOR



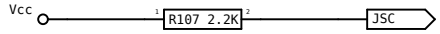


* (2) Pe cablajul original JEXA/9
era legat la o via care nu ducea
nicaieri mai departe.
In schemele originale JEXA/9 era
legat la un semnal SI/TRG3 care
nu exista nicaieri in alta parte.
Pe placa mea veche JEXA/9
este legat la NVS.
(Vezi legatura #24 fata 2)

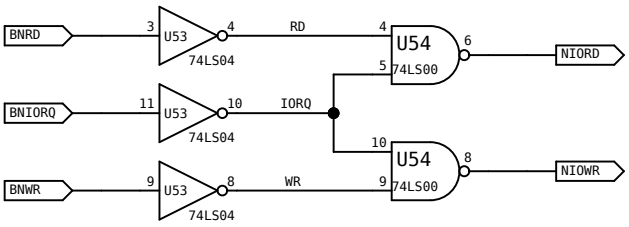
* (2) On the original mainboard, JEXA/9 was connected
to a via which was not further leading anywhere.
In the original schematics, JEXA/9 was connected to
a signal "SI/TRG3" which did not exist anywhere else.
On my old mainboard, JEXA/9 is connected to NVS.
(See rewiring #24 side 2)



* (3) Pe cablajul original, R107 este legata
in mod gresit la GND in loc de VCC.
(Vezi taietura #13 fata 1, legatura #19 fata 2)

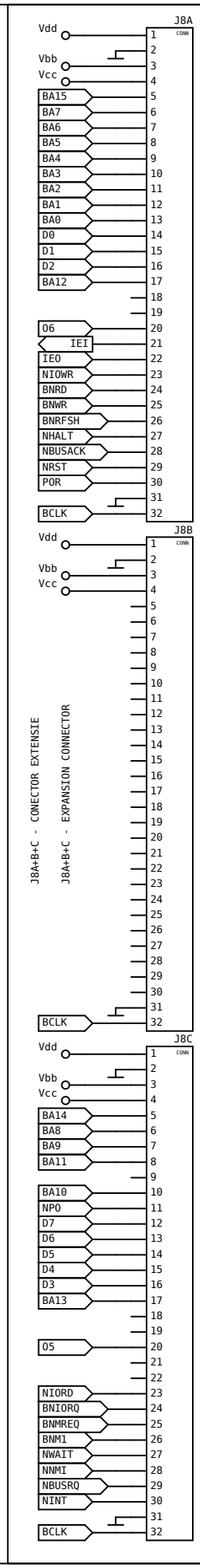


* (3) On the original mainboard, R107 is
wrongfully connected to GND instead of VCC.
(See cut #13 side 1, rewiring #19 side 2)

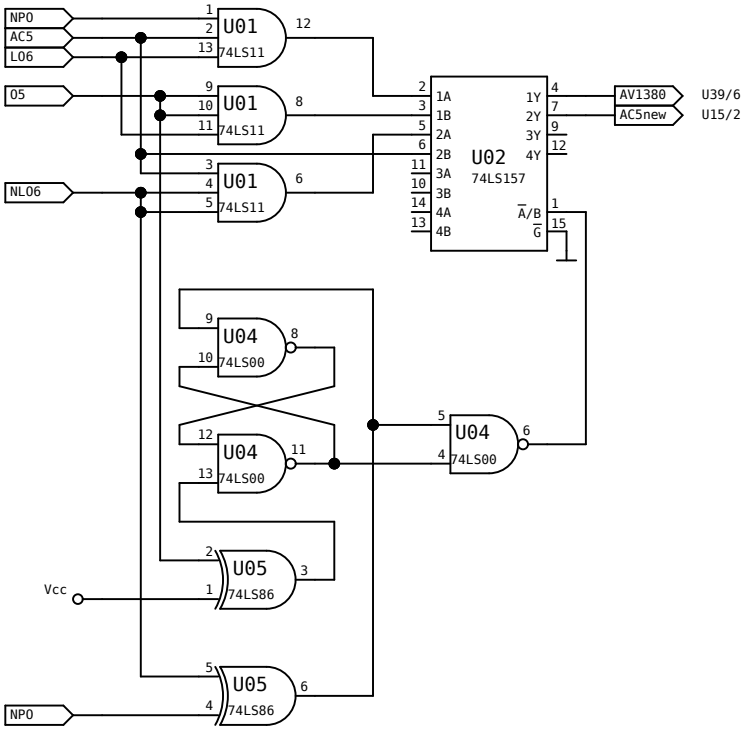


* (4) Cablajul original avea JSC conectat
la J6/pin10 dar manualul original avea JSC
listat la J6/pin8. Am schimbat cablajul placii
de baza pentru a corespunde manualului.
(Vezi taietura #5 fata 1, legatura #1 fata 1)

* (4) The original mainboard had JSC connected
to J6/pin10 but the original manual had JSC
listed at J6/pin8. I changed the mainboard layout
to match the original manual.
(See cut #5 side 1, rewiring #1 side 1)

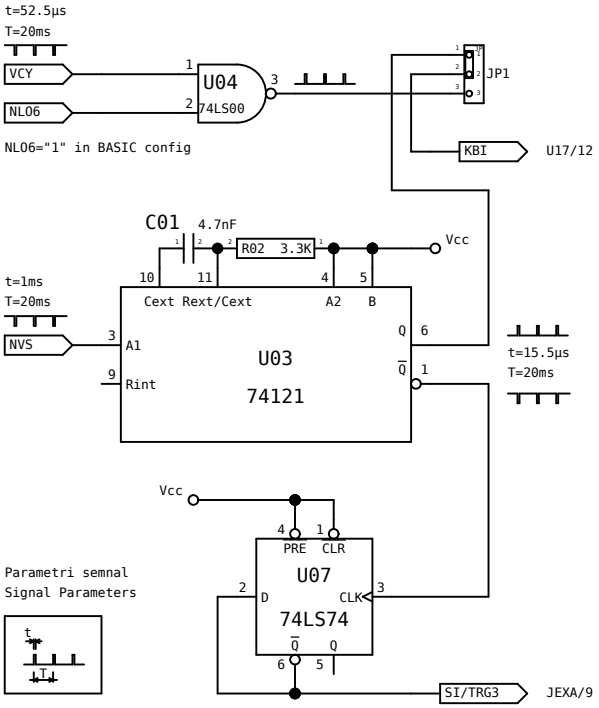


TITLE	µC CoBra - Interfete CoBra µC - Interfaces		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	14 OF 17	DRAWN BY:	ElectroNNix



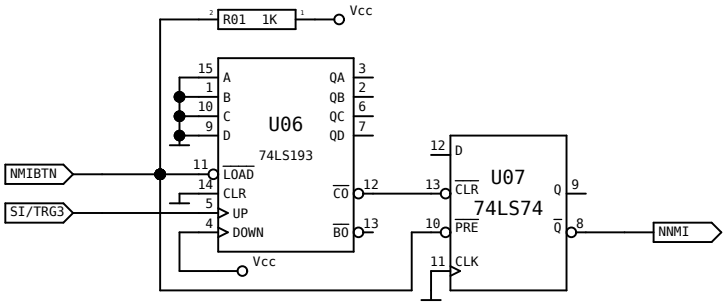
Circuit modificare 80 caractere pe linie

80 characters per line modification circuit



Circuit generator intreruperi

Interrupt generator circuit



Circuit generator semnal NMI

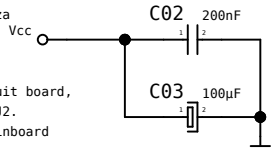
NMI generator circuit

* (2) Circuitul de mai sus (generator intreruperi), furnizeaza semnalul de intrerupere cu perioada de 20 ms specific Spectrum (KBI) care este mai departe aplicat intrarii U17/12 (7400) de pe placa de baza.
Din JP1 se poate alege pentru KBI fie solutia din schema originala ($\overline{VCY \times LO6}$), fie semnalul generat la U75/6.
NOTA: Cablajul imprimat original avea intrarea U17/12 legata la intrarea U17/5, care intrare era legata la semnalul VLD. Deci versiunea originala folosea semnalul VLD ca semnal de intreruperi Basic Spectrum.
Versiunea 0.2 de placa de baza cu care functioneaza modulul prezentat aici are prevazut un jumper (JP20), din care se poate alege ca semnal de intreruperi Spectrum fie VLD (de pe placa de baza) fie KBI (generat aici).

Acest circuit mai furnizeaza si intreruperile pentru interfata de floppy disk (semnalul SI/TRG3) care este aplicat pe placa de baza la pinul 9 al conectorului de interfata floppy (JEXA/9).
NOTA: Cablajul imprimat original al placii de baza avea JEXA/9 neconectat, datorita unui traseu lipsa pe cablajul placii de baza, ceea ce nu permitea functionarea interfetei de disc. Placa mea de baza veche (verde) avea JEXA/9 conectat la NVS, iar cea gri avea JEXA/9 conectat la semnalul SI/TRG3 generat ca mai sus.
Versiunea de placa de baza cu care modulul prezentat pe aceasta pagina functioneaza are prevazut un jumper, din care se poate alege ca semnal de intreruperi pentru interfata floppy fie NVS fie SI/TRG3 (generat aici).

* (1) Circuitele de pe aceasta pagina se afla pe o placa de circuit imprimat separata, care se cupleaza la placa de baza prin conectorii J1 si J2.
J1/J2 se infig in conectorii J12/J13 de pe placa de baza.

* (1) Circuits on this page are located on a separate circuit board, which is connected to the mainboard through connectors J1/J2.
J1/J2 are to be inserted into connectors J12/J13 on the mainboard

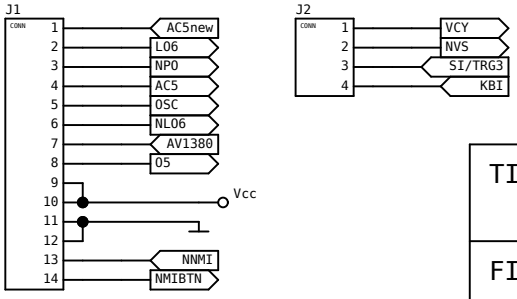


* (2) The circuit above (Interrupt Generator), provides the 20 ms interrupt signal specific to Spectrum (KBI) which is further applied to input U17/12 (7400) on the mainboard. JP1 can choose between a KBI signal generated according to the original schematic (VCY xor LO6) and the output of U75/6.
NOTE: The original mainboard had input U17/12 connected to input U17/5, which was further connected to VLD. So the original version used VLD as interrupt signal for Spectrum Basic.
The mainboard version (0.2) used in conjunction with the module described on this page is designed with a jumper (JP20), which can select either VLD (from the mainboard) or KBI (generated here) as the Spectrum Basic interrupt signal.

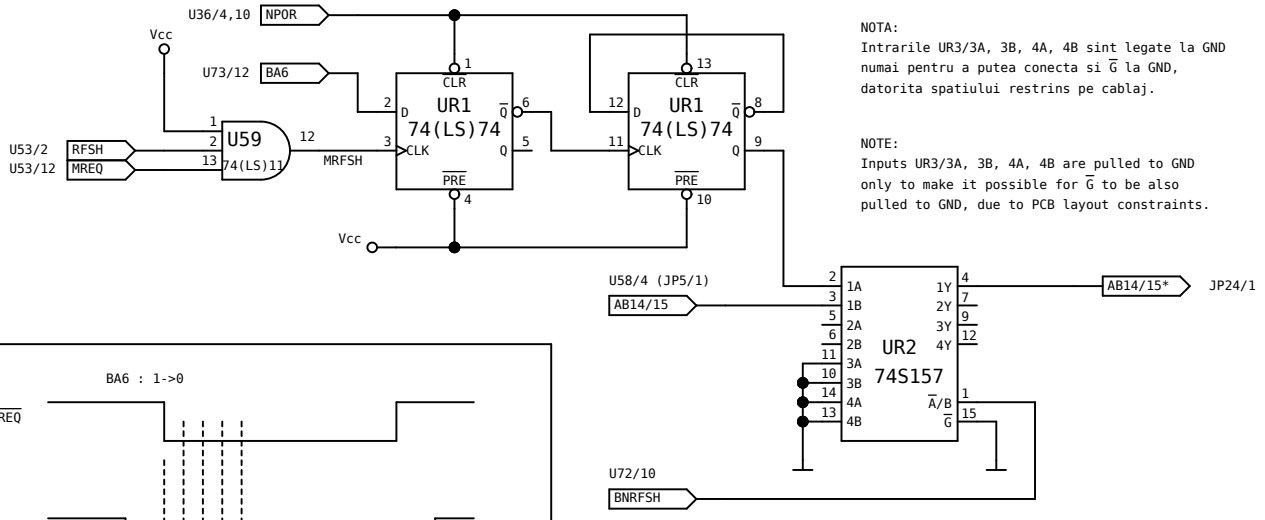
This circuit also provides the interrupts to the floppy disk interface (signal SI/TRG3) which is applied to pin 9 of the floppy interface connector (JEXA/9) on the mainboard.
NOTE: The original mainboard had JEXA/9 left disconnected due to a missing connection on the printed circuit board, which rendered the floppy interface unusable. My old mainboard (green) had JEXA/9 connected to NVS, and the grey one had JEXA/9 connected to signal SI/TRG3 generated as above.
The mainboard version used in conjunction with the module described on this page is designed with a jumper, which can select either NVS (from the mainboard) or SI/TRG3 (generated here) as the interrupt signal for the floppy interface.

J1, J2 - Conectori modul modificari

J1, J2 - Modif. module connectors

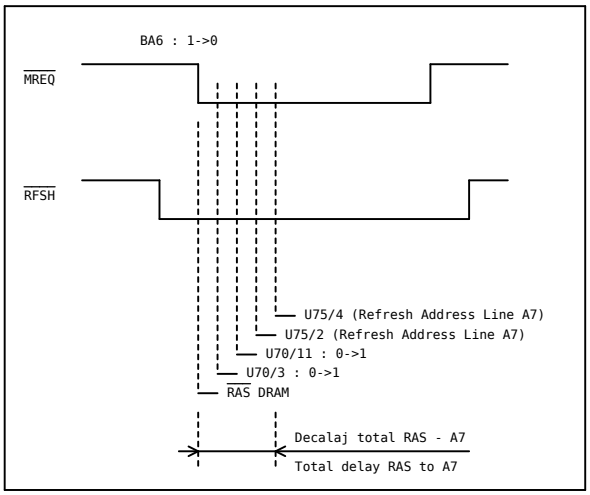


TITLE	Modulul cu circuite de modificari Modifications module		
FILE:	CoBra	REVISION:	0.4a
PAGE	15 OF 17	DRAWN BY:	ElectroNNix



NOTA:
Intrarile UR3/3A, 3B, 4A, 4B sint legate la GND
numai pentru a putea conecta si $\overline{G}$ la GND,
datorita spatiului restrins pe cablaj.

NOTE:
Inputs UR3/3A, 3B, 4A, 4B are pulled to GND
only to make it possible for $\overline{G}$ to be also
pulled to GND, due to PCB layout constraints.



NOTE:

Due to the physical constraints related to the construction of the printed circuit board, the CPU address lines are not connected to the address inputs of the memories in the same order, but they are shuffled.
Thus, the correspondence between CPU address lines and the system memory address inputs (during refresh) is the following:

CPU Address	Memory Address
BA0	A0
BA1	A6
BA2	A1
BA3	A2
BA4	A3
BA5	A4
BA6	A5
AB14	A7

NOTA:

Datorita constringerilor fizice de realizare ale cablajului imprimat, liniile de adresa de la procesor nu sint legate in ordinea normala la intrarile de adrese ale memoriilor, ci amestecat.
Astfel, corespondenta intre linii de adresa procesor si linii adresa memorii sistem (pe durata refresh-ului) este:

Adrese CPU	Adrese memorii
BA0	A0
BA1	A6
BA2	A1
BA3	A2
BA4	A3
BA5	A4
BA6	A5
AB14	A7

Operation:

The diagram above shows the CPU refresh cycle corresponding to the changing of refresh address from 127 (7Fh, 1111111) to 0 (0000000) i.e. the change of refresh address bit 6 from 1 to 0. This change is detected by the circuit presented which "builds" the bit 7 of the refresh address by dividing the frequency of CPU refresh address bit A6 by 2.

In order to sample the CPU refresh address line BA6 correctly, a logical AND between signals MREQ and RFSH is used (signals already existing on the mainboard, generated by inverting $\overline{\text{MREQ}}$ and $\overline{\text{RFSH}}$) since the CPU refresh address lines are only guaranteed stable during $\overline{\text{MREQ}}$ activation (and $\overline{\text{RFSH}}$ of course).

The diagram above shows the consecutive delays through the 2 flip-flops and the multiplexer, as well as the delay of signal MREQ x RFSH from the falling edge of $\overline{\text{MREQ}}$, delay due to the inverters which generate signals MREQ and RFSH and due to gate U59/12.

Considering that the falling edge of $\overline{\text{MREQ}}$ is used as a RAS signal to the memory, all these delays cumulated add up to a total delay of the refresh addres bit A7 which is pretty significant.

Basically at the moment the refresh address changes from 127 to 0, bit A7 "produced" here for the 8-bit refresh address will not go from 0 to 1 soon enough to be part of the next logical refresh address (128).
Therefore the sequence of the refresh addresses generated will be:

128, 1, ... 127, 0, 129, ... 254, 255, 128, 1, ...

but this will still NOT affect the correct operation of the memory because the maximum refresh period will still be satisfied for all rows of the DRAM cell matrix.

Functionare:

Diagrama alaturata prezinta ciclul de refresh generat de procesor corespunzator schimbarii adresei de refresh de la 127 (7Fh, 1111111) la 0 (0000000) adica schimbarii bitului 6 de adresa refresh din 1 in 0. Aceasta schimbare este detectata de circuitul prezentat care "confectioneaza" bitul 7 de adresa refresh prin divizare cu 2 a frecventei liniei A6 de adresa pentru refresh de la procesor.

Pentru a esantiona corect linia de adresa BA6 de la procesor folosita pentru refresh se foloseste un SI logic intre MREQ si RFSH (semnale deja existente pe placa de baza, obtinute prin inversarea $\overline{\text{MREQ}}$ si $\overline{\text{RFSH}}$) intrucit liniile de adresa sint garantate stabile doar pe perioada activarii $\overline{\text{MREQ}}$.

In diagrama alaturata sint reprezentate intirzierile succesive prin cei doi bistabili si prin multiplexor, precum si intirzierea semnalului MREQ x RFSH fata de frontul negativ al $\overline{\text{MREQ}}$, intirziere datorata inversoarelor care genereaza MREQ si RFSH precum si portii U59/12.

Avind in vedere ca frontul negativ al $\overline{\text{MREQ}}$ este folosit ca semnal de RAS pentru memorie, toate aceste intirzieri cumulate provoaca o intirziere totala destul de semnificativa a bitului A7 de adresa pentru refresh.

Practic la momentul schimbarii adresei de refresh din 127 in 0, bitul A7 "confectionat" aici pentru adresa refresh pe 8 biti nu va trece din 0 in 1 suficient de rapid pentru a intra in componenta urmatoarei adrese de refresh (128).
Deci succesiunea adreselor de refresh generate va fi:

128, 1, ... 127, 0, 129, ... 254, 255, 128, 1, ...

dar asta nu va afecta buna functionare a memoriei intrucit tot se va respecta perioada maxima de refresh pentru toate liniile matricei de celule de memorie.

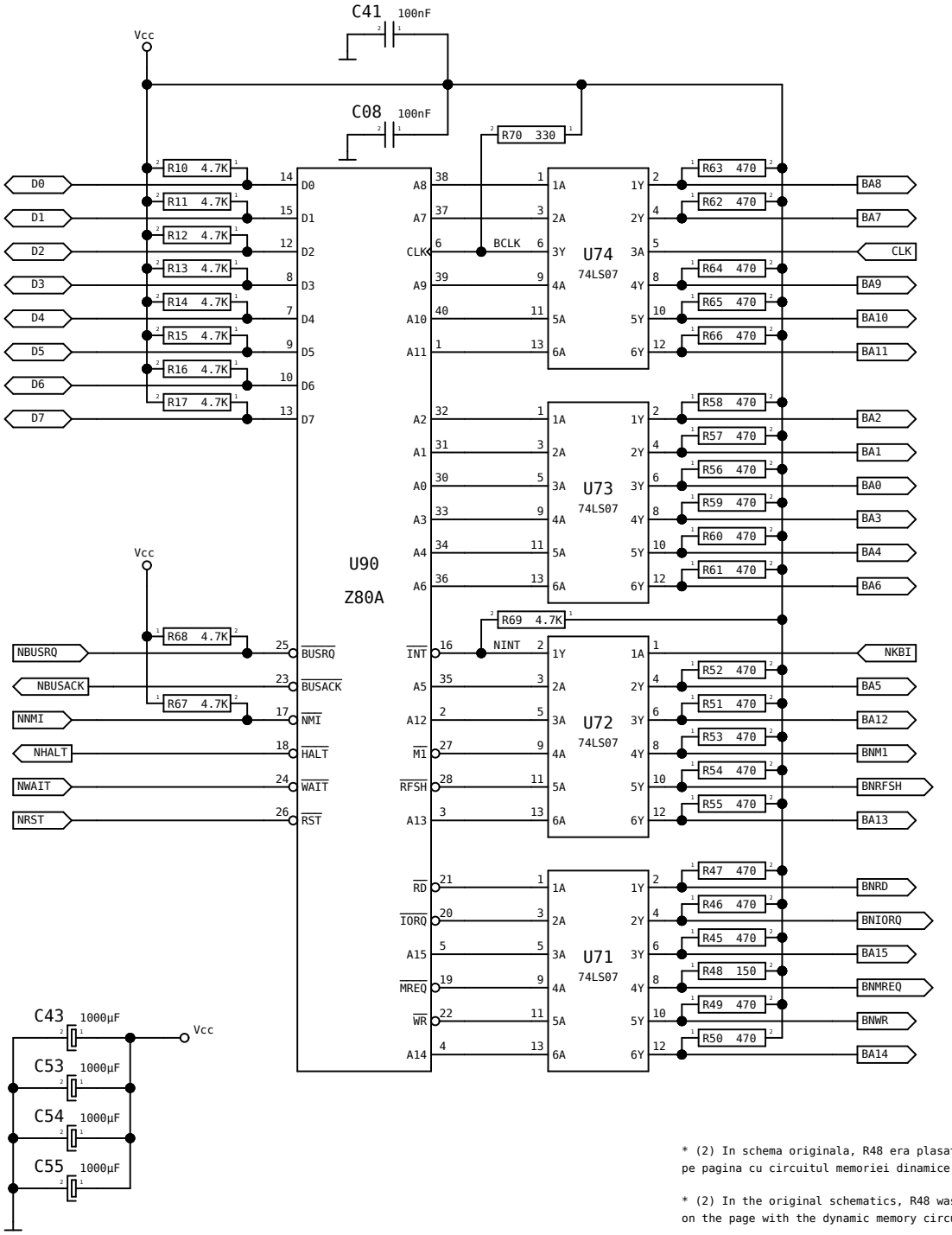
TITLE	µC CoBra - Refresh RAS-Only pe 8 biti CoBra µC - 8-bit RAS-Only Refresh		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	16 OF 17	DRAWN BY:	ElectroNNix

* (2) In practica am folosit rezistente de 470 Ohm (in loc de 680 Ohm ca in schema originala) pentru a obtine niste semnale de adrese de putere ceva mai mare.

* (2) In actuality I used 470 Ohm resistors (instead of 680 Ohm as in the original schematics) in order to have address line signals a little more powerful.

* (1) In schema originala, U74/6 era legat (gresit) la U90/24, dar corect este ca U90/24 sa fie legat la NWAIT, U74/6 (BCLK) sa fie legat la U90/6 (CLK procesor) si U74/5 sa fie legat la CLK

* (1) In the original schematics, U74/6 was connected (wrong) to U90/24, but correct is for U90/24 to be connected to NWAIT, for U74/6 (BCLK) to be connected to U90/6 (CPU clock) and for U74/5 to be connected to CLK

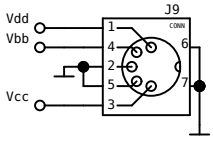


* (2) In schema originala, R48 era plasata pe pagina cu circuitul memoriei dinamice.

* (2) In the original schematics, R48 was drawn on the page with the dynamic memory circuit.

J9 - CONECTOR ALIMENTARE

J9 - POWER CONNECTOR



TITLE	µC CoBra - Unitatea centrala CoBra µC - Central Processing Unit		
FILE:	CoBra	REVISION:	3.17e (test, 64/80KB DRAM)
PAGE	17 OF 17	DRAWN BY:	ElectroNNix